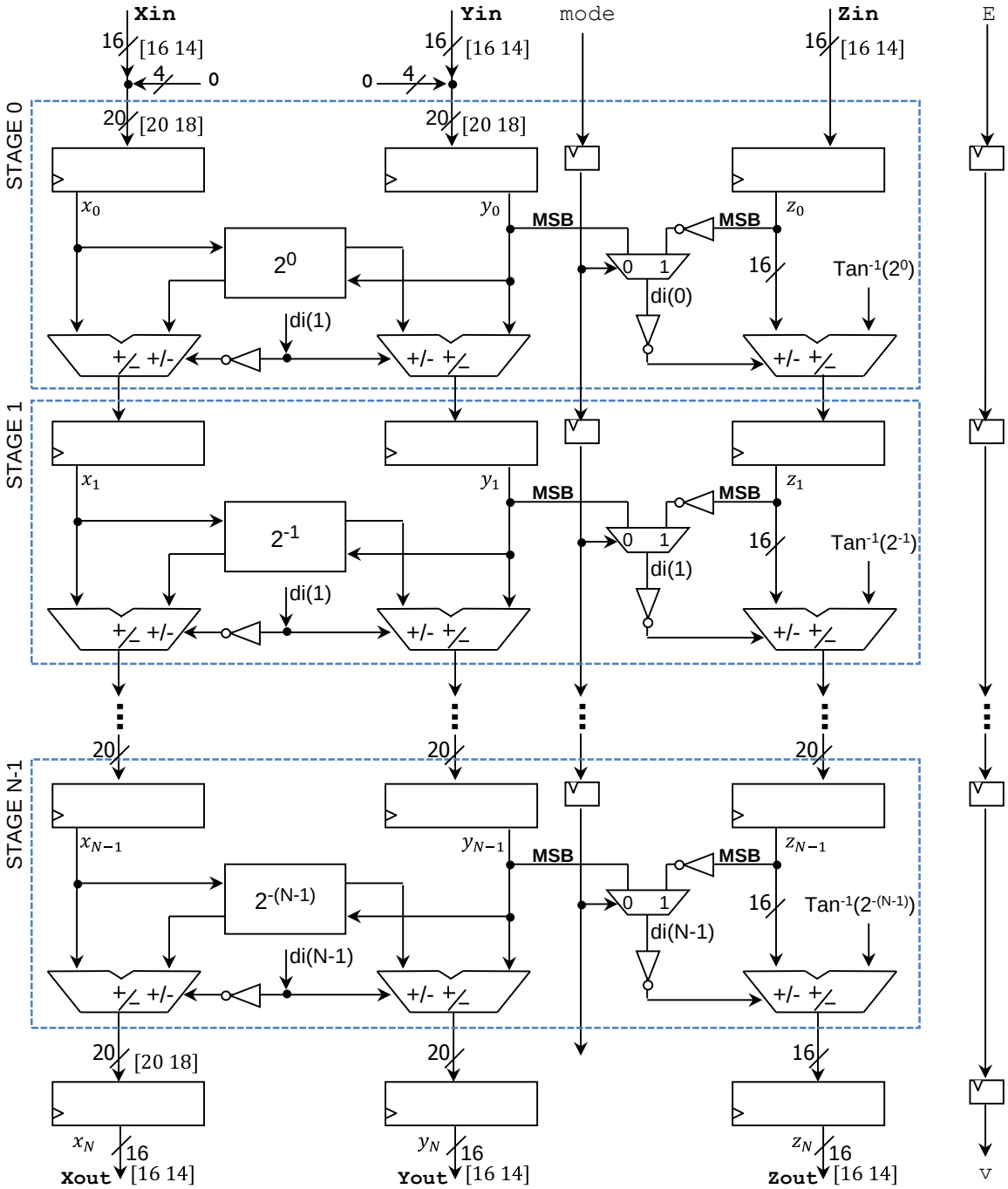
Homework 4

(Due date: November 18th @ 7:30 pm)

Presentation and clarity are very important! Show your procedure!

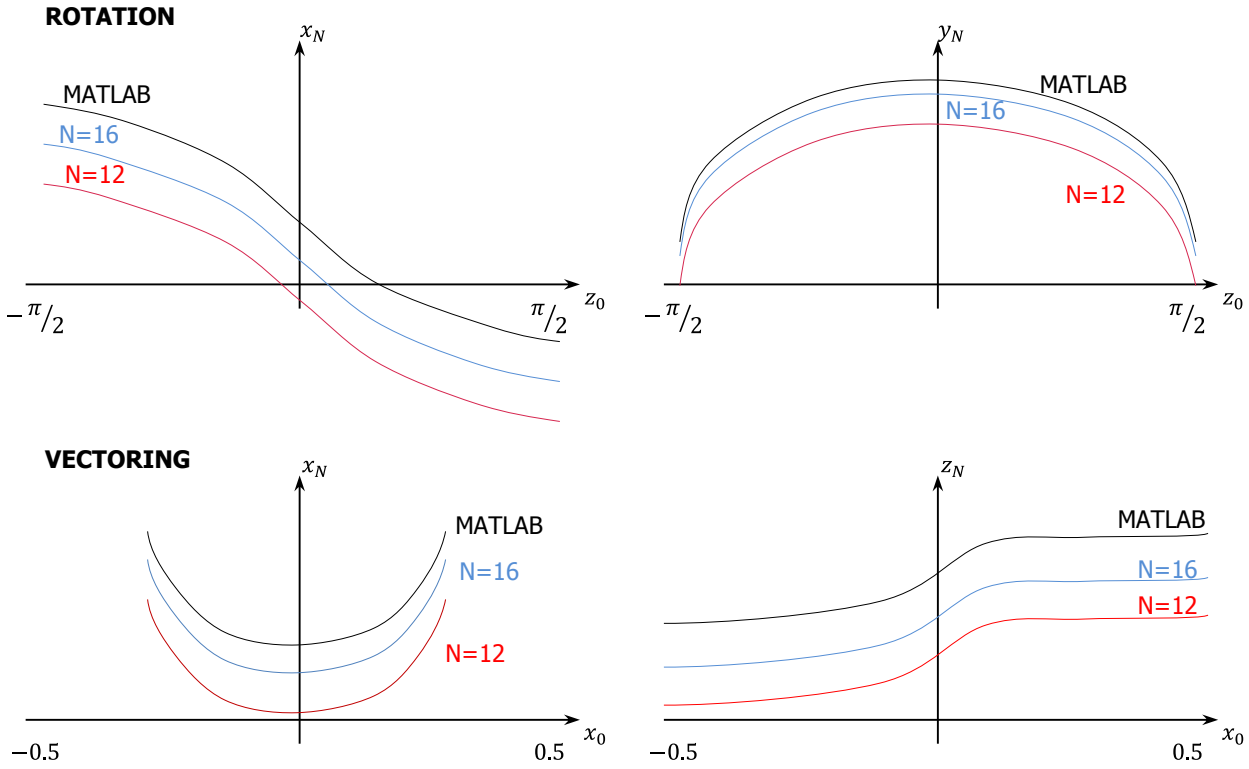
PROBLEM 1 (60 PTS)

- Design the pipelined Circular CORDIC architecture with N iterations shown in the figure below.
- The circuit must have N as a parameter. $N = 4\ to\ 16$.
- Attach a printout of your VHDL code.



PROBLEM 2 (40 PTS)

- Create a testbench to test your CORDIC circuit. The testbench should test the following cases for $N = 12$ and $N = 16$.
  - ✓ Rotation Mode: $x_0 = 0, y_0 = 1/A_n, z_0 = -\pi/2 \ to \ \pi/2$. For z_0, we test 100 equally-spaced values between $-\pi/2 \ to \ \pi/2$.
  - ✓ Vectoring Mode: $y_0 = 1, z_0 = 0, x_0 = -0.5 \ to \ 0.5$. For x_0, we test 100 equally-spaced values between $-0.5 \ to \ 0.5$.
- Your testbench must write the output results in a text file.
- MATLAB® (or Octave): Read data from the testbench output file and plot the results (for $N = 12, 16$ and for rotation and vectoring mode) with the results of the functions to which the CORDIC results converge (use MATLAB®).
- **Important considerations**:
  - ✓ The CORDIC algorithm in the vectoring mode for Z tends to: $z_n = z_0 + atan2(y_0, x_0)$. This is not exactly the arctangent function.
  - ✓ Keep in mind the range of convergence: for some arguments, the CORDIC results might not converge to the expected function (MATLAB®) values. The figure below is just referential.



- Attach a printout of your: i) VHDL testbench, ii) input text file for testbench, iii) output text file from testbench.